IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application	)	PATENT APPLICATION
Inventors: Rashid, et al.	)	
Application No.: Unknown	)	
Filed Date: December 21, 2001	)	
Title: CROSS-BAR SWITCH EMPLOYING A MULTIPLE ENTRY POINT FIFO	)	Customer No.: 28554

PRELIMINARY AMENDMENT

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Applicants respectfully request that the Examiner enter the following amendments to the above-identified patent application, which is a continuation of U.S. Patent Application Serial No. 09/900,514, assigned to Group Art Unit 2661.

AMENDMENTS

Please amend the application as follows:

In the Claims:

Please replace claims 1-38 with claims 39-79 as shown below. Applicants add new claims 39-79 and cancel claims 1-38. All pending claims are reproduced below.

39. (new) An apparatus comprising:

a plurality of inputs;

a FIFO storage buffer;

request logic coupling said plurality of inputs to said FIFO storage buffer; and

a memory in communication with said request logic, wherein said memory is adapted to concurrently maintain a plurality of pointers, wherein each pointer in said plurality of pointers corresponds to a different location in said FIFO storage buffer for storing data from an input port in said set of input ports.

40. (new) The apparatus of claim 39, wherein said memory includes:

a first entry adapted to maintain a pointer corresponding to a first location in said FIFO storage buffer for storing a first set of data from an input port in said set of input ports; and

a second entry adapted to maintain a pointer corresponding to a second location in said FIFO storage buffer for storing a second set of data from an input port in said set of input ports.

41. (new) The apparatus of claim 40, wherein said memory includes:

a third entry adapted to maintain a pointer corresponding to a third location in said FIFO storage buffer for storing a third set of data from an input port in said set of input ports; and

a fourth entry adapted to maintain a pointer corresponding to a fourth location in said FIFO storage buffer for storing a fourth set of data from an input port in said set of input ports.

42. (new) The apparatus of claim 39, wherein said memory is adapted to maintain a data identifier for each pointer in said plurality of pointers.

43. (new) The apparatus of claim 42, wherein each data identifier identifies a data source.

44. (new) The apparatus of claim 39, wherein said memory is a content addressable memory.

45. (new) The apparatus of claim 39, wherein said request logic and said storage buffer are included in a multiple port memory.

46. (new) An apparatus comprising:

a plurality of inputs;

a FIFO storage buffer;

request logic coupling said plurality of inputs to said FIFO storage buffer; and

a memory in communication with said request logic, wherein said memory is adapted to concurrently maintain a plurality of pointers, wherein each pointer in said plurality of pointers corresponds to a different location in said FIFO storage buffer for storing data from an input port in said set of input ports,

wherein said memory is adapted to maintain a data identifier for each pointer in said plurality of pointers, wherein each data identifier identifies a data source, and

wherein said memory includes:

a first entry adapted to maintain a pointer corresponding to a first location in said FIFO storage buffer for storing a first set of data from an input port in said set of input ports, and

a second entry adapted to maintain a pointer corresponding to a second location in said FIFO storage buffer for storing a second set of data from an input port in said set of input ports.

47. (new) The apparatus of claim 46, wherein said memory includes:

a third entry adapted to maintain a pointer corresponding to a third location in said FIFO storage buffer for storing a third set of data from an input port in said set of input ports; and

a fourth entry adapted to maintain a pointer corresponding to a fourth location in said FIFO storage buffer for storing a fourth set of data from an input port in said set of input ports.

48. (new) The apparatus of claim 46, wherein said memory is a content addressable memory.

49. (new) The apparatus of claim 46, wherein said request logic and said storage buffer are included in a multiple port memory.

50. (new) A sink port comprising:

a plurality of data inputs;

a multiple entry point FIFO having a plurality of inputs in communication with said plurality of data inputs to accept and store data; and

an output port coupled to said multiple entry point FIFO to receive said data from said storage buffer and transmit said data on a communications link.

51. (new) The sink port of claim 50, wherein said multiple entry point FIFO includes:

a FIFO storage buffer;

request logic coupling said plurality of data inputs to said FIFO storage buffer; and

a memory in communication with said request logic, wherein said memory is adapted to concurrently maintain a plurality of pointers, wherein each pointer in said plurality of pointers corresponds to a different location in said FIFO storage buffer for storing data from an input port in said set of input ports.

52. (new) The sink port of claim 51, wherein said memory includes:

a first entry adapted to maintain a pointer corresponding to a first location in said FIFO storage buffer for storing a first set of data from an input port in said set of input ports; and

a second entry adapted to maintain a pointer corresponding to a second location in said FIFO storage buffer for storing a second set of data from an input port in said set of input ports.

53. (new) The sink port of claim 52, wherein said memory includes:

a third entry adapted to maintain a pointer corresponding to a third location in said FIFO storage buffer for storing a third set of data from an input port in said set of input ports; and

a fourth entry adapted to maintain a pointer corresponding to a fourth location in said FIFO storage buffer for storing a fourth set of data from an input port in said set of input ports.

54. (new) The sink port of claim 51, wherein said memory is adapted to maintain a data identifier for each pointer in said plurality of pointers.

55. (new) The sink port of claim 54, wherein each data identifier identifies a data source.

56. (new) The sink port of claim 51, wherein said memory is a content addressable memory.

57. (new) The sink port of claim 51, wherein said request logic and said storage buffer are included in a multiple port memory.

58. (new) A cross-bar switch comprising:

a set of input ports to receive data packets; and

a set of sink ports in communication with said set of input ports to accept and forward said data packets, wherein a first sink port in said set of sink ports includes:

a multiple entry point FIFO having a plurality of data inputs adapted to store data from data packets accepted by said first sink port.

59. (new) The cross-bar switch of claim 58, wherein said multiple entry point FIFO includes:

a FIFO storage buffer;

request logic coupling said plurality of data inputs to said FIFO storage buffer; and

a memory in communication with said request logic, wherein said memory is adapted to concurrently maintain a plurality of pointers, wherein each pointer in said plurality of pointers corresponds to a different location in said FIFO storage buffer for storing data from an input port in said set of input ports.

60. (new) The cross-bar switch of claim 59, wherein said memory includes:

a first entry adapted to maintain a pointer corresponding to a first location in said FIFO storage buffer for storing a first set of data from an input port in said set of input ports; and

a second entry adapted to maintain a pointer corresponding to a second location in said FIFO storage buffer for storing a second set of data from an input port in said set of input ports.

61. (new) The cross-bar switch of claim 60, wherein said memory includes:

a third entry adapted to maintain a pointer corresponding to a third location in said FIFO storage buffer for storing a third set of data from an input port in said set of input ports; and

a fourth entry adapted to maintain a pointer corresponding to a fourth location in said FIFO storage buffer for storing a fourth set of data from an input port in said set of input ports.

62. (new) The cross-bar switch of claim 59, wherein said memory is adapted to maintain a data identifier for each pointer in said plurality of pointers.

63. (new) The cross-bar switch of claim 62, wherein each data identifier identifies a data source.

64. (new) The cross-bar switch of claim 59, wherein said memory is a content addressable memory.

65. (new) The cross-bar switch of claim 59, wherein said request logic and said storage buffer are included in a multiple port memory.

66. (new) The cross-bar switch of claim 58, wherein each sink port in said set of sink ports includes:

a multiple entry point FIFO having a plurality of data inputs.

67. (new) The cross-bar switch of claim 58 further including:

a set of data rings in communication with said set of input ports and said set of sink ports.

68. (new) The cross-bar switch of claim 67, wherein said multiple entry point FIFO includes a data input for each data ring in said set of data rings.

69. (new) The cross-bar switch of claim 67, wherein said first sink port snoops data packets on each data ring in said set of data rings and determines whether to accept a first data packet based on a set of criteria, wherein said set of criteria includes:

said first sink port having sufficient storage space for storing said first data packet,

said first sink port supporting a destination targeted by said first data packet, and

a total number of packets being received by said first sink port not exceeding a predetermined number of packets.

70. (new) The cross-bar switch of claim 67, wherein said first sink port includes:

a ring interface coupled to said set of data rings to accept data from a plurality of sources and supply said data on a plurality of outputs;

said multiple entry point FIFO in communication with said plurality of outputs on said ring interface to receive and store said data from said ring interface; and

an output port coupled to said multiple entry point FIFO to receive data from said multiple entry point FIFO and transmit said data from said multiple entry point FIFO on a communications link.

71. (new) A method for a sink port in a cross-bar switch to collect data in a FIFO, said method comprising the steps of:

(a) accepting data from a first data packet, wherein said data accepted in aid step (a) is a subset of said first data packet;

(b) storing said data from said first data packet in a said FIFO;

(c) accepting data from a second data packet, wherein said data accepted in aid step (c) is a subset of said second data packet;

(d) storing said data from said second data packet in said FIFO.

72. (new) The method of claim 71, wherein said first data packet originates from a first source and said second data packet originated from a second source.

73. (new) The method of claim 71, further including the steps of:

(e) determining that said data accepted in said step (a) includes a first line of said first data packet;

(f) allocating a first location in said FIFO for storing data from said first data packet;

(g) determining that said data accepted in said step (c) includes a first line of said second data packet; and

(h) allocating a second location in said FIFO for storing data from said second data packet.

74. (new) The method of claim 73, wherein said step (f) includes the steps of:

(1) creating a first pointer to said first location; and

(2) creating a first tag identifying said first data packet.

75. (new) The method of claim 74, wherein said step (h) includes the steps of:

(1) creating a second pointer to said second location; and

(2) creating a second tag identifying said second data packet.

76. (new) The method of claim 75, wherein said first tag identifies a source of said first data packet and said second tag identifies a source of said second data packet.

77. (new) The method of claim 73, further including the steps of:

(j) accepting additional data for said first data packet;

(k) determining that said additional data accepted in said step (j) does not includes a first line of said first data packet;

(l) identifying a position in said first location in said FIFO for storing said additional data from said first data packet;

(m) accepting additional data for said second data packet;

(n) determining that said additional data accepted in said step (m) does not includes a first line of said second data packet; and

(o) identifying a position in said second location in said FIFO for storing said additional data from said second data packet.

78. (new) The method of claim 77,

wherein said step (l) includes the step of:

(1) retrieving a pointer to said position in said first location, and

wherein said step (o) includes the step of:

(2) retrieving a pointer to said position in said second location.

79. (new) The method of claim 73, further including the steps of:

(p) accepting additional data for said first data packet;

(q) determining that said additional data accepted in said step (p) includes a last line of said first data packet;

(r) purging a pointer to a position in said first location in said FIFO;

(s) accepting additional data for said second data packet;

(t) determining that said additional data accepted in said step (r) includes a last line of said second data packet; and

(u) purging a pointer to a position in said second location in said FIFO.

In the Specification:

Please replace the title of the above-identified patent application appearing at page 1, line 1 of the application with the title appearing below. A marked up copy of the amended title is shown in Appendix A to this Amendment.

CROSS-BAR SWITCH EMPLOYING A MULTIPLE ENTRY POINT FIFO

In the Abstract:

Please replace the ABSTRACT of the above-identified patent application appearing at page 43 of the application with the ABSTRACT appearing below. A marked up copy of the amended ABSTRACT is shown in Appendix B to this Amendment.

A cross-bar switch includes a set of input ports for receiving data packets and a set of sink ports coupled to the input ports to accept and forward the data packets. Each sink port includes a multiple entry point FIFO with multiple data inputs for receiving data packets. In one implementation, the multiple entry point FIFO includes a FIFO storage buffer and request logic coupling the multiple entry point FIFO's data inputs to the FIFO storage buffer. The multiple entry point FIFO concurrently maintains separate pointers into the FIFO storage buffer for each data packet being received on the multiple entry point FIFO's data inputs.

REMARKS

Applicants respectfully submit that claims 39-79 are in order for allowance and request consideration of these claims.

The Commissioner is authorized to change any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this document.

Respectfully submitted,

Date: December 21, 2001

By: _____
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APPENDIX A

The title of the patent application appearing at page 1, line 1 of the application has been amended as follows:

CROSS-BAR SWITCH EMPLOYING A MULTIPLE ENTRY POINT FIFO

APPENDIX B

The ABSTRACT of the patent application appearing at page 43 of the application has been amended as follows:

[A cross-bar switch includes a set of input ports for receiving data packets and a set of sink ports for transmitting the received packets to identified targets. A set of data rings couples the input ports to the sink ports. Each sink port utilizes the set of data rings to simultaneously accept multiple data packets targeted to the same destination — creating a non-blocking cross-bar switch. Sink ports are also each capable of supporting multiple targets — providing the cross-bar switch with implicit multicast capability.]

A cross-bar switch includes a set of input ports for receiving data packets and a set of sink ports coupled to the input ports to accept and forward the data packets. Each sink port includes a multiple entry point FIFO with multiple data inputs for receiving data packets. In one implementation, the multiple entry point FIFO includes a FIFO storage buffer and request logic coupling the multiple entry point FIFO's data inputs to the FIFO storage buffer. The multiple entry point FIFO concurrently maintains separate pointers into the FIFO storage buffer for each data packet being received on the multiple entry point FIFO's data inputs.